What is claimed is:

1. A precharge system, appropriate for an active matrix display device having a plurality of data lines, a plurality of scan lines, a plurality of pixels, a first voltage source, and a second voltage source, comprising a precharge circuit having:

a plurality of first transistors, having gate electrode and drain electrode connected together to function as a diode, of which a first terminal is coupled to the first voltage source;

a second transistor of which a first terminal is coupled to the second terminals of the first transistors, of which a second terminal is coupled to the data lines, and a control terminal receives a positive precharge signal;

a plurality of third transistors, having gate electrode and drain electrode connected together to function as a diode, of which a first terminal is coupled to the second voltage source; and

a fourth transistor of which a first terminal is coupled to the second terminals of the third transistors, of which a second terminal is coupled to the corresponding data lines, and a control terminal receives a negative precharge signal.

2. The precharge system as claimed in claim 1, wherein the first transistors are N-type thin film transistors.

3. The precharge system as claimed in claim 1, wherein the second transistor is an N-type thin film transistor.

4. The precharge system as claimed in claim 1, wherein the second transistor is a P-type thin film transistor.

5. The precharge system as claimed in claim 1, wherein the third transistors are N-type thin film transistors.

6. The precharge system as claimed in claim 1, wherein the third transistors are P-type thin film transistors.

7. The precharge system as claimed in claim 1, wherein the first transistors are P-type thin film transistors.

8. The precharge system as claimed in claim 1 further comprising a plurality of precharge circuits coupled to the corresponding data lines.

9. The precharge system as claimed in claim 8 further comprising a control signal generation circuit for generating the positive precharge signal and the negative precharge signal.

10. The precharge system as claimed in claim 9, wherein the control signal generation circuit comprises:

a selection circuit having an input terminal, a selection terminal, a complementary selection terminal, a first output terminal, and a second output terminal, wherein the input terminal receives a start impulse signal and the selection terminal and the complementary selection terminal enable the first output terminal or the second output terminal; and

a voltage level shifter for receiving a clock signal and a complementary clock signal and for coupling the clock signal and the complementary clock signal respectively to the selection terminal and to the complementary selection terminal.

11. The precharge system as claimed in claim 9, wherein the control signal generation circuit comprises:

a selection circuit having an input terminal, a selection terminal, a complementary selection terminal, a first output terminal, and a second output terminal, wherein the input terminal receives a start impulse signal and wherein the selection terminal and the complementary selection terminal enable the first output terminal or the second output terminal; and

a voltage level shifter for receiving the common voltage signal and coupling the amplified common voltage signal and the complementary amplified common voltage signal respectively to the selection terminal and to the complementary selection terminal.

an inverter of which an input terminal is coupled to the output terminal of the voltage level shifter and an output terminal is coupled to the complementary selection terminal.

12. The precharge system as claimed in claim 11, wherein the selection circuit comprises:

a first transmission gate having a first terminal and a second terminal, wherein the first terminal is coupled to the input terminal and wherein a first gate of the second terminal is coupled to the selection terminal, and a second gate of the second terminal is coupled to the complementary selection terminal;

a third transistor having a first terminal coupled to the second terminal of the first transmission gate, having a second terminal coupled to a low voltage source, and having a control terminal coupled to the selection terminal;

a second transmission gate having a first terminal and a second terminal, wherein the first terminal is coupled to the input terminal and wherein a first gate of the second terminal is coupled to the complementary selection terminal, and a second gate of the second terminal is coupled to the selection terminal; and

a fourth transistor having a first terminal coupled to the second terminal of the second transmission gate, having a second terminal coupled to the low

voltage source, and having a control terminal coupled to the complementary selection terminal.

13. The precharge system as claimed in claim 8 further comprising a plurality of control signal generation circuits for respectively generating the positive precharge signal and the negative precharge signal and for coupling the positive precharge signal and the negative precharge signal to the corresponding precharge circuits.